International Journal of Applied Mathematics and Computin6 Science. Volume 7, Issue 1, (2023) 23-29
http://www.cayley-nielson.com/ijamcs

# A Distributed Fieldbus Technology for Generator Excitation System Data Storage Design

**Jingtao Yin**
School of Electronic Technology and Engineering, Shanghai Technical Institute of Electronics & Information, Shanghai , China
**E-mail:** *yinjingtao@126.com*

**Abstract**

In this study is the use of the generator excitation system design parameters for distributed fieldbus technology and real-time data display module record, will transfer to the field bus data processing and real-time storage of a design. Generator current and terminal voltage and other electrical parameters by the CAN bus pass, when a failure occurs, the fault current and other electrical parameters display, and store it to MRAM or FRAM memory, and also through the external communications port to be transferred to PC and other networks. System uses magnetic resistance random access memory, ferroelectric memory extends the storage capacity, so that fault recording function can be achieved; application PIT and RTC, the timing accuracy of a millisecond, improve the recording wave function.

**Keywords:** Fieldbus; MRAM; FRAM; SPI module; fault recorder

## 1. Introduction

With computer technology, automation technology continues to develop and field bus such as CAN bus technology has improved, the excitation control system gradually to a distributed Fieldbus direction. The design of excitation system parameters of real-time data recording and display module is part of generator excitation control an important part of the excitation control system reflects the decentralized control, centralized key information. Complete on-site data, and easy to modify the parameters of fault recorder. The system needs to support large-capacity power-down to save memory used to store fault switching and analog to be used after the fault display and analysis, which uses ferroelectric random access memory storage and magneto-resistance [1].

## 2. Magnetoresistance Random Access Memory

### 2.1. Magnetoresistive random access memory principle introduced

MRAM is a non-volatile magnetic random access memory. MRAM uses magnetic storage elements in each tunnel junction (MTJ) devices for data storage. When the bias applied to the MTJ, the magnetic polarization of the electrons is called tunneling through (Tunneling) process, through insulating barrier. When the free layer magnetic moment parallel to the fixed layer, MTJ devices with low resistance; and when the free layer and fixed layer magnetization direction antiparallel (anti-parallel), then a high resistance. With the magnetic state changes the device, the resistance will change its data as a magnetic state (rather than charge) storage, and by measuring the resistance to induction, does not interfere with the magnetic state [2].

### 2.2. Magnetoresistance random access memory applications

Designed with Freescale Semiconductor to provide the magnetoresistance random access memory MR2A16A, used to store a variety of electrical excitation system parameters.Pin functions shown in Table 1:

Table.1 MR2A16A Pin-out diagram

| Signal Name | Function |
|---|---|
| A[17:0] | Address Input |
| $\overline{E}$ | Chip Enable |
| $\overline{W}$ | Write Enable |
| $\overline{G}$ | Output Enable |
| $\overline{UB}$ | Choose High-byte |
| $\overline{LB}$ | Choose low-byte |
| DQL[7:0] | Data I / O high byte |
| DQU[15:8] | Data I / O low byte |
| VDD | +3.3V Supply voltage |
| VSS | Ground |
| NC | No connection |

| | | | | |
|---|---|---|---|---|
| $\overline{RE}$ | O | — | — | Read Enable, indicates external read access |
| ADDR[22:20] | O | T | — | External address |
| ACC[2:0] | O | | — | Access source |
| ADDR[19:16] | O | T | — | External address |
| IQSTAT[3:0] | O | | — | Instruction Queue Status |
| ADDR[15:1] | O | T | — | External address |
| IVD[15:1] | O | | — | Internal visibility read data (IVIS = 1) |
| ADDR0 | O | T | F | External address |
| IVD0 | O | | | Internal visibility read data (IVIS = 1) |
| $\overline{UDS}$ | O | — | | Upper Data Select, indicates external access to the high byte DATA[15:8] |
| $\overline{LSTRB}$ | O | — | F | Low Strobe, indicates valid data on DATA[7:0] |
| $\overline{LDS}$ | O | — | | Lower Data Select, indicates external access to the low byte DATA[7:0] |
| R/$\overline{W}$ | O | — | F | Read/Write, indicates the direction of internal data transfers |
| $\overline{WE}$ | O | — | | Write Enable, indicates external write access |
| DATA[15:8] | I/O | — | — | Bidirectional data (even address) |
| DATA[7:0] | I/O | — | — | Bidirectional data (odd address) |
| $\overline{EWAIT}$ | I | — | — | External control for external bus access stretches (adding wait states) |

Fig. 1 External bus interface

### 2.3. External expansion bus

MCU and external expansion bus on the pin shown in Figure 1. This design uses a separate 16-bit data bus DATA [15,0] and 18-bit address bus ADDR [18,1], external expansion memory mapped address 0x20_0000 to 0x27CFFF, a total of 512Kbyte. MCU's connection with MR2A16A shown in Figure 2.

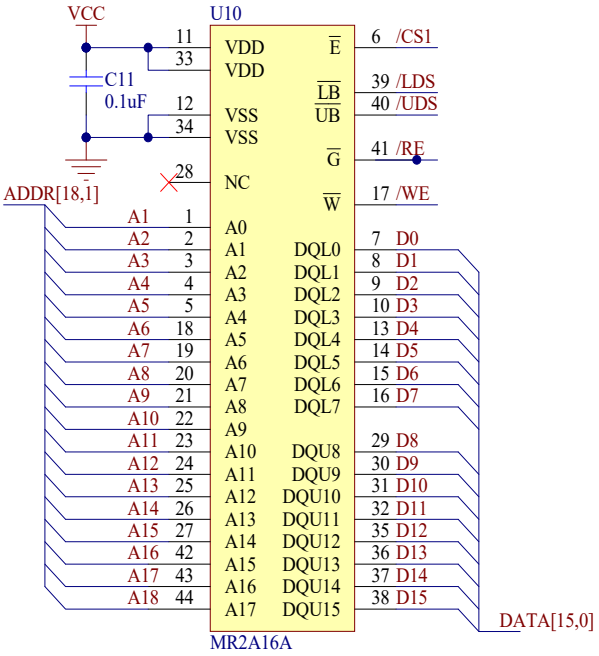


Fig.2 External memory connection on large module

MCU through the following steps to complete a read operation: drive / CS1, drive ADDR, / UDS & / LDS, driver / RE, wait, read data from the DATA line, recovery / RE, recovery / CS1, / UDS & / LDS .

MCU through the following steps to complete a read operation: drive / CS1, drive ADDR, / UDS & / LDS, DATA bus driver, drivers / WE, wait, resume / WE, resume / CS1, / UDS & / LDS.

Write programs to simply define a variable external address, and then treat as ordinary variables operate on the external variables can be completed in external memory read and write.

## 3. Ferroelectricity Memory

### 3.1. Basic working principle of memory

When an electric field is added to the ferroelectric crystal, the central atom in the crystal along the direction of the field move. When the atom moves, it is through an energy barrier, causing the charge breakdown. Sensing circuit to charge the internal breakdown and set the memory. After removal of the electric field, the central atom to remain intact, the memory state is preserved. FRAM does not require regular updating, the data can continue to save after power-down, fast and not easy to write bad.

### 3.2. Ferroelectric memory applications

The system uses Ramtron's FM25L256, used to store the time stamp and the corresponding switch.

FRAM can be the same as the RAM read and write operations at bus speed of completion, because it is not charge to store data but with the work in the polarization state, so without waiting for the data is written,

there is no write delay, but also like a traditional non-volatile volatile memory as to provide non-volatile storage. You can save data up to ten years, more simple to use, improve the reliability of the system. With the same high-speed RAM, also supports virtually unlimited number of read and write cycles. These advantages make the functions of RAM and ROM technologies in a single chip[3]. FM25L256 function block diagram (Figure 3) and the pin menu (Table 2) as follows:

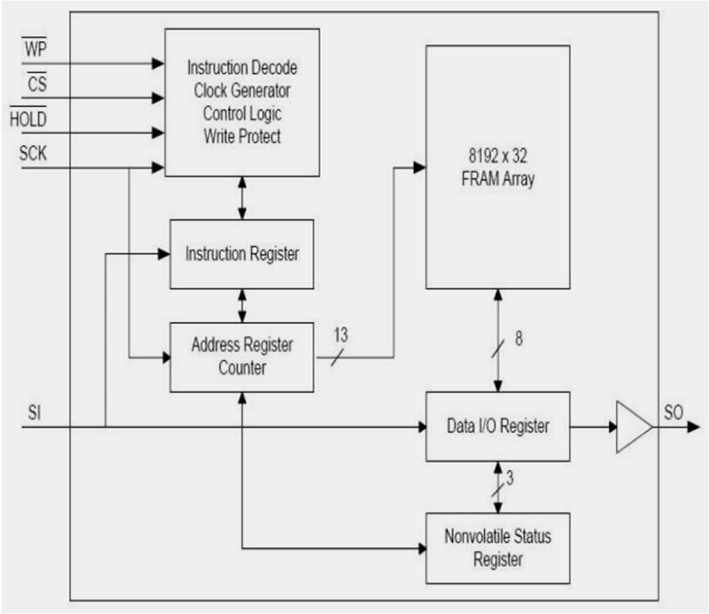


Fig.3 FM25L256Function

Table.2 FM25L256 Pin-out block chart

| Pin Name | Function |
|---|---|
| /CS | Chip Select |
| /WP | Write Protect |
| /HOLD | Keeping |
| SCK | Serial Clock |
| SI | Serial Data Input |
| SO | Serial Data Output |
| VDD | Supply Voltage (2.7V ~ 3.6V) |
| VSS | Ground |

**3.3. SPI module works**

FM25L256 connected with the microcontroller through the SPI bus. Figure 4 shows the wiring diagram of the SPI bus. Host (SCM) in the 8-bit data register and the slave (FM25L256) in the 8-bit data register through the MOSI and MISO to form a distributed 16-bit shift register. In the data transmission process, the data in both input and output serial manner. According to the host to provide the serial clock synchronization signal, the data through two data lines between the master and slave cyclic shift, the host data register data to the data from the machine registers, and slave data register in data transmission to the

host data register. SPI module is achieved in this way between master and slave data exchange.

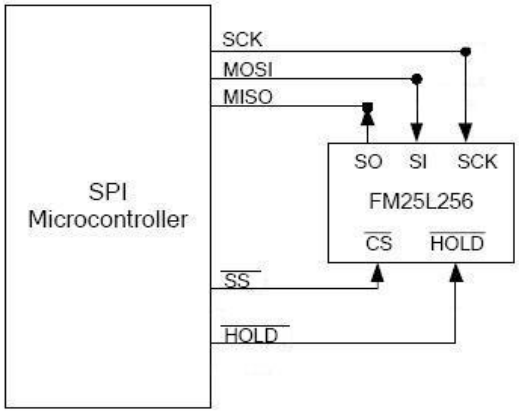


Fig.4 SPI bus connection

SPI interface, the transmission mode can be set SPICR1 CPOL and CPHA in the two to control. Support mode 0 and 3 modes of these two models. Figure 5 shows the timing of these two models:

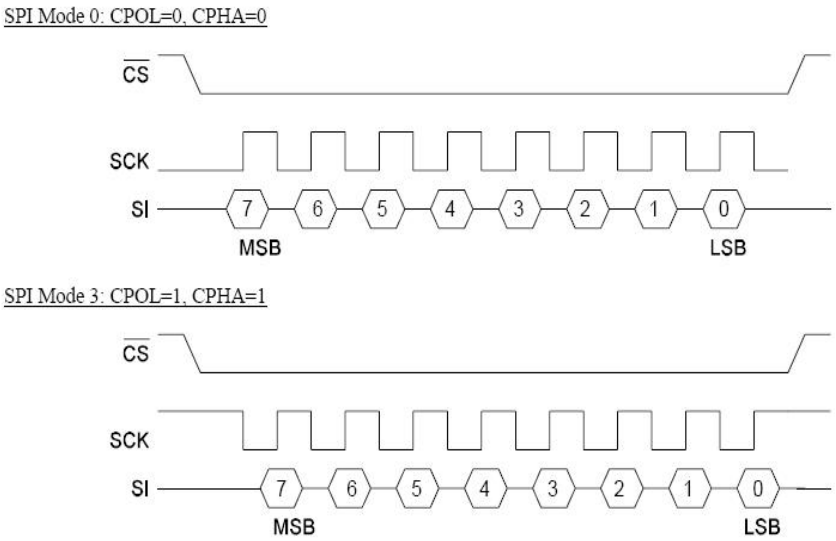


Fig.5 mode 0&3 of SPI bus

**3.4. SPI software program designed to**

In this system, SPI work in host mode 3. Following completion of the program mainly includes the SPI initialization.

```
void initial_SPI1（void）
{
        SPI1CR1 = 0x5E；
        SPI1CR2 = 0x10；
        SPI1BR   = 0x22；
}
```

Read mainly access the data stored in FM25L256 write operation is to collect the data to FM25L256 in the specified location. SPI read and write the specific procedure is described below.

Read: read the first function to determine whether to enter into after reading the status register SPI0SR, to determine whether the data register is empty, empty read data command is sent, sent after reading the status register SPI0SR, to determine whether the data register is empty, sending empty high address, read status register until the transmission is completed SPI0SR, to determine whether the data register is empty, empty, send low address, read status register until the transmission is completed SPI0SR, determine the data register is empty, if it is empty at this time, read data register , the read is complete.

Writes: First write a function to determine whether to enter into after reading the status register SPI0SR, to determine whether the data register is empty, empty send write enable command, after reading the status register after a delay SPI0SR, to determine whether the data register is empty, empty send high address, read status register until the transmission is completed SPI0SR, to determine whether the data register is empty, empty, send low address, read status register until the transmission is completed SPI0SR, determine the data register is empty at this time, if empty, send data , the write operation is completed.

## 4. Time Tag

For this system, accurate and rapid transmission on the CAN bus to the storage of data is very important, and accurate data transfer to the recording time is also very important, this time to be accurate to the millisecond. No time recorded data is incomplete. The system uses the DS3234, and the PIT with the MCU's internal record of the time to complete the millisecond time stamp[4].

## 5. Conclusion

This module reflects the excitation control system to control the spread of information focused on trends, to achieve the required system functions: MCU's on-site analysis of the received data to determine fault. When a fault occurs, the data stored in memory or ferroelectric random access memory in the magnetic resistance, and add millisecond time stamp. Users can view any failures of the electrical parameters of voltage waveform.

This design has been discussed by the laboratory verification, real viable solution. The object of study not only for the excitation system, and can be applied to other areas of industrial control, such as a variety of instrumentation, a variety of monitoring systems, as long as the content of slightly modified design, or by a combination of individual modules can be simple for a variety of systems, so that the system has a strong practicality and versatility.

## Acknowledgement

This research is supported by Senior Talent Program of Shanghai Technical Institute of Electronics & Information GCC2023001.

## References

[1] Zhou Zhigang, Wang Yun-bo, Wang Hua. Ferroelectric memory research. Information Recording Materials, 2002: Vol.3, No.1

[2] Meng Chen, Li Min. FM24C256 high-performance ferroelectric memory and its applications in single-chip. Electronic Technology, 2003: No.1

[3] Sun Shu-printed. Ferroelectric memory compare theory and application. Microcontroller and embedded system applications,2004.9:15-18

[4] Gu Wenfeng. Human-computer interface design research. Luoyang University, 1999, Vol.14 No4 :55-56

[5] Queiroz, J. C., Santos, Y. T., da Silva, I. C., & Farias, C. T. (2021). Damage Detection in Composite Materials Using Tap Test Technique and Neural Networks. Journal of Nondestructive Evaluation, 40(1), 27.

[6] El-amiri, A., Mokhliss, H., Saifi, A., Halloua, H., Obbadi, A., Errami, Y., ... & Elhassnaoui, A. (2018, December). Infrared thermography detection of flex cracks in multi-layer ceramic capacitors (MLCCs). In 2018 6th International Renewable and Sustainable Energy Conference (IRSEC) (pp. 1-5). IEEE.

[7] Tsai, T. H., Jeyaprakash, N., & Yang, C. H. (2020). Non-destructive evaluations of 3D printed ceramic teeth: Young's modulus and defect detections. Ceramics International, 46(14), 22987-22998.

[8] Sakamoto, F., Takahashi, T., Tatami, J., & Iijima, M. (2019). Prediction of strength based on defect analysis in Al2O3 ceramics via non-destructive and three-dimensional observation using optical coherence tomography. Journal of the Ceramic Society of Japan, 127(7), 462-468.

[9] Ikhlef, B., Rahmoune, C., Toufik, B., & Benazzouz, D. (2021). Gearboxes fault detection under operation varying condition based on MODWPT, Ant colony optimization algorithm and Random Forest classifier. Advances in Mechanical Engineering, 13(8), 16878140211043004.

[10] Afia, A., Rahmoune, C., Benazzouz, D., Merainani, B., & Fedala, S. (2021). New gear fault diagnosis method based on modwpt and neural network for feature extraction and classification. Journal of Testing and Evaluation, 49(2), 1064-1085.